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[REDACTED] ART UNIT      [REDACTED] PAPER NUMBER

2124

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BEFORE THE BOARD OF PATENT APPEALS

AND INTERFERENCES

Page No. 11

Application Number: 09/432,337

Filing Date: November 2, 1999

Appellant(s): Acharya

MAILED  
JUN 24 2003  
Technology Center 2100

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Fred G. Pruner, Jr.

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed April 17, 2003.

**(1) Real Party in Interest**

A statement identifying the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have bearing on the decision in the pending appeal is contained in the brief.

Art Unit: 2124

**(3) Status of Claims**

The statement of the status of the claims contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Invention**

The summary of invention contained in the brief is correct.

**(6) Issues**

The appellant's statement of the issues in the brief is correct.

**(7) Grouping of Claims**

Appellant's brief includes a statement that claims 1-3 and 9-11 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

**(8) ClaimsAppealed**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(9) Prior Art of Record**

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

Art Unit: 2124

**(10) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-3 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lesthievent et al.

**Claim 1**

1. a chain of processing units ..., each processing unit being associated with one of a group of filter coefficients;
2. a tap selection circuit to select a group of the processing units of the chain to produce and indication of a filtered discrete output value for each discrete input value.

**Lesthievent et al.'s Fig. 4**

1. a filter architecture has Q physical stages which are considered as the claimed “chain of processing units”. Each unit has “N” stages, wherein  $1 < N < Q$ . The filter coefficients  $g(0)$ - $g(Q-1)$  are divided to “N” and considered as the claimed “group of filter coefficients”;
2. switches  $S(0)-S(Q-1)$  which are capable of connecting the input  $X(W)$  and delayed inputs  $X(W-1)-X[W-(Q-1)]$  to corresponding multipliers for producing an output  $y(n)$ .

It is noted that Lesthievent et al do not specifically detail the claimed “tap selection circuit”; however, the switches  $S(i)$  are capable of providing the equivalent function, i.e., select a group of processing units having multipliers “ $g(i)$ ”. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to design the claimed invention according to Lesthievent et al’s teachings because the reference is a digital filter having selecting features as claimed.

Art Unit: 2124

As per dependent claim 2, the claim adds the “systolic chain”. According to applicant’s specification, page 3, lines 22-25, the “systolic architecture” means the “chain of processing units” produce a “different output value on each clock cycle”. Lesthievent et al’s “processing units having multipliers g(i)” do the same.

As per dependent claim 3, the switch s(i) are capable of selecting number of “processing units having multipliers g(i)”.

As per dependent claims 9-10, the detail features are old and well known in the art.

As per dependent claim 11, Lesthievent et al’s filter is FIR filter.

#### **(11) *Response to Argument***

The thrust of the Appellant’s position that:

**(A)** “[i]n summary, Lesthievent fails to show a tap selection circuit, and the examiner fails to show any support for the alleged suggestion or motivation to modify Lesthievent to dirive the missing tap selection circuit”,

**(B)** “[c]laim 3 depends from independent claim 1 and recites that the tap selection circuit selects a number of taps of the processing circuit”,

**(C)** “[t]he processing circuit of claim 9 depends from the independent claim 1 and recites that the tap selection circuit includes a register that stores bits indicateive of the processing units in the group” and

**(D)** “[c]laim 10 dependends from the independent claim 1 and recites that each processing unit includes a register that stores an indication of an associated filter coefficient” (emphasis added).

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With respect to the **arguments**, the examiner carefully reviews and analyzes the **claimed invention** and applied reference.

(A) First, the claimed “**tap selection circuit to select a group of the processing units**” feature, as interpreted by examiner, is merely “selecting” a group of processing units. Lesthievent et al’s Fig. 4 **does** show the claimed feature. For example, Q physical stages divided in “N” processing units. The **switches S(0)-S(Q-1) are capable of connecting/disconnecting the input X(W) and delayed inputs X(W-1)-X[W-(Q-1)]** to provide the desired **output y(n) which is result of selected processing unit(s)**. It is noted that Lesthievent et al **does** show the sample-and-hold mechanism” (col. 4, lines 52-55), i.e., the delays “z” and the “switches S(i)”. It is also noted that the “delay” “z” is a interchanged term for “tap” in the filter art. Therefore, Lesthievent et al’s **the delays “z” and switches are capable of performing the equivalent function of Appellant’s “tap selection circuit to select a group of the processing units”**,

(B) Second, although Lesthievent does NOT disclose the phrase “**tap selection circuit**” in the patent, the examiner believes that the combined **delays “z” and switches “S(i)”** are providing the equivalent function as claimed in dependent claim 3,

(C) Third, because the **switches “S(i)”** have the control signals for **connecting/disconnecting** the input X(W) and delayed inputs X(W-1)-X[W-(Q-1)], storage means should store the information of control signals. Therefore, it would have been obvious to obvious to a person having ordinary skill in the art at the time the invention was made to use a register that stores bits as claimed in the Lesthievent’s filter, and

(D) Fourth, if the filter has a plurality of processing units, the filter coefficients for each

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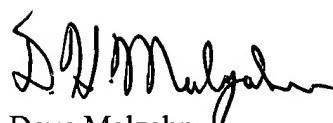
processing unit are different. The information, as claimed, should stored in the memory means.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,



TAN V. MAI  
PRIMARY EXAMINER



Dave Malzahn  
Primary Examiner, as conferee



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June 23, 2003

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